
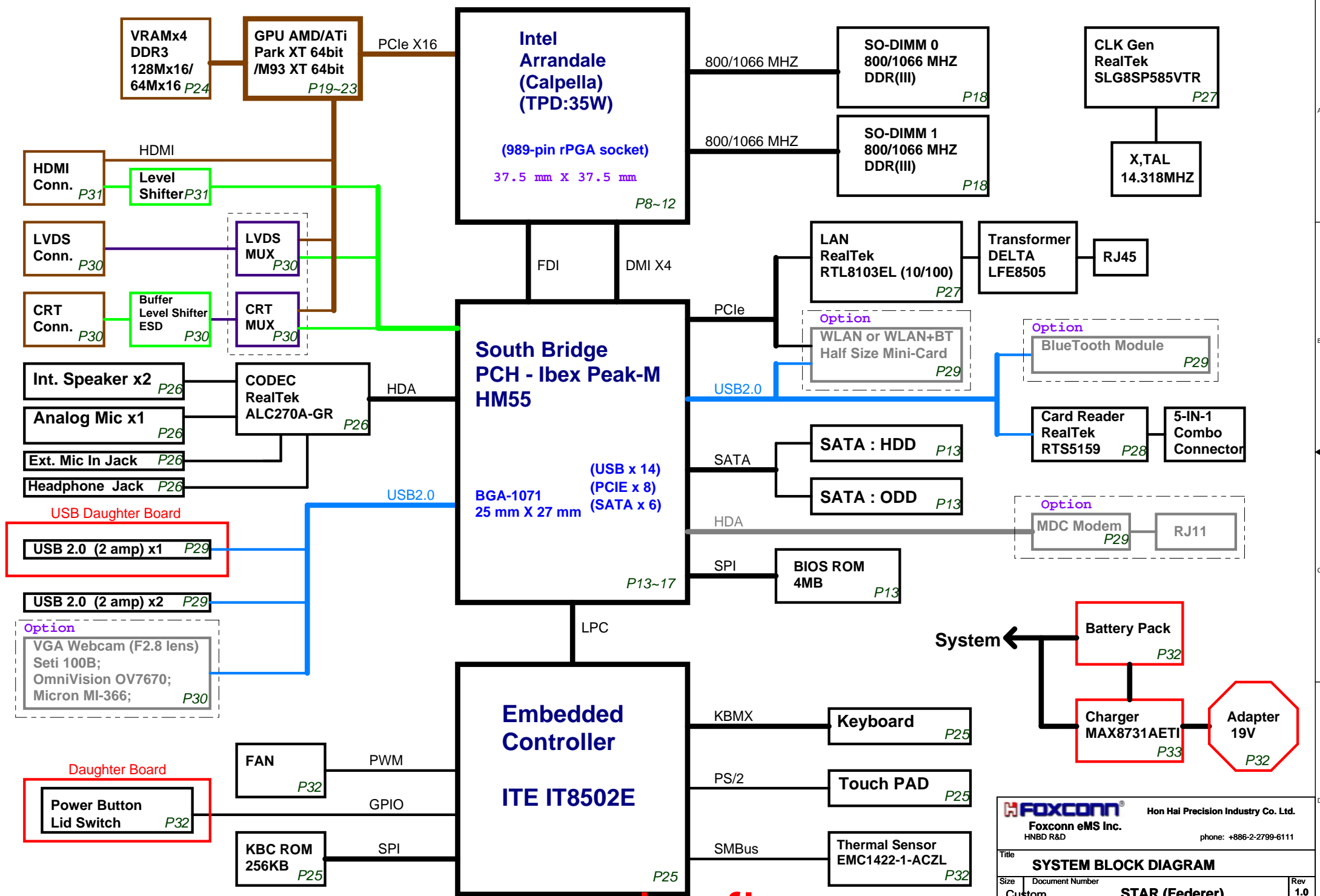
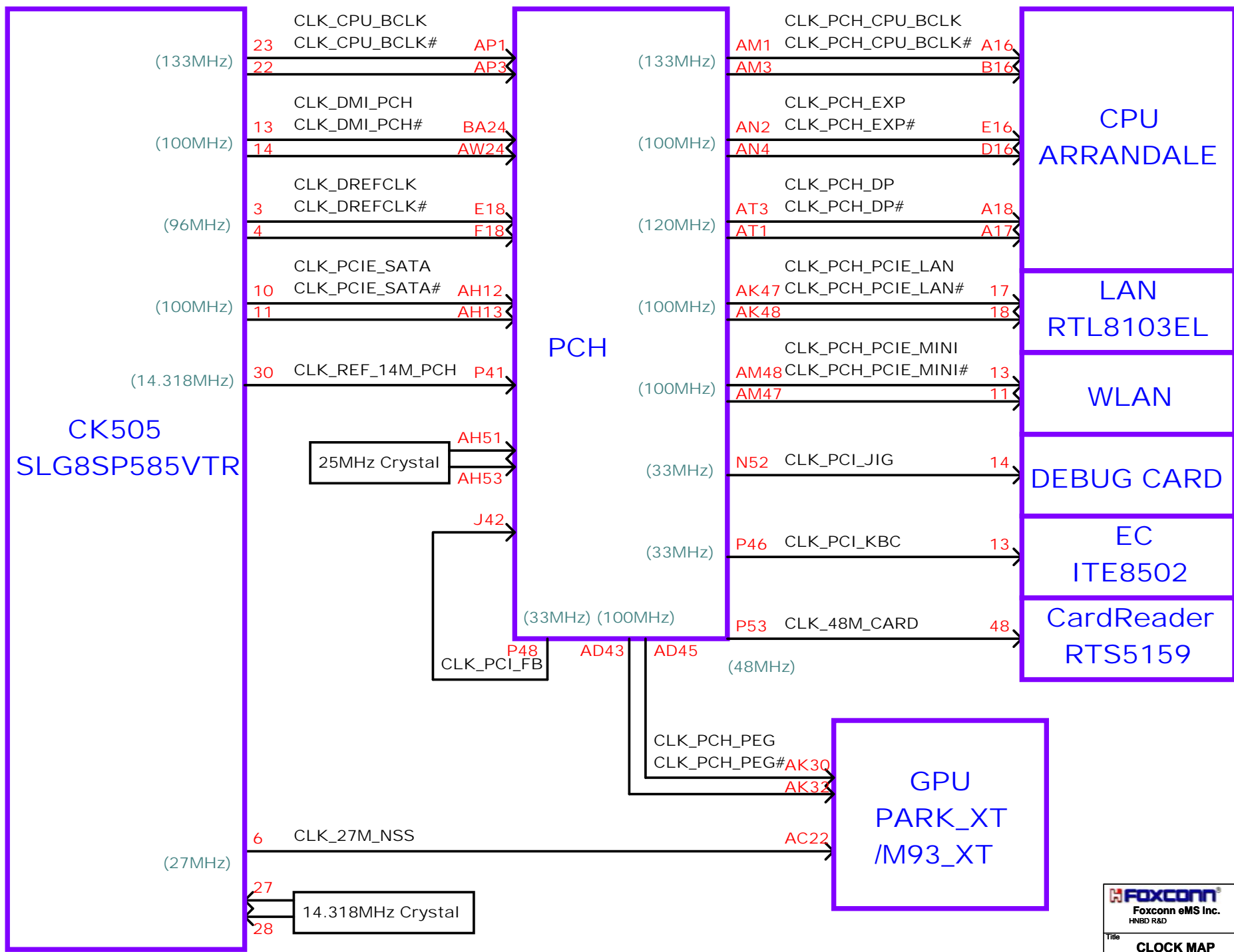


01 -- COVER SHEET	21 -- VGA_S3 (DDR3) 3/5
02 -- SYSTEM BLOCK DIAGRAM	22 -- VGA_S3 (DP) 4/5
03 -- CLOCK MAP	23 -- VGA_S3 (POWER) 5/5
04 -- POWER MAP	24 -- VRAM (DDR3)
05 -- POWER SEQUENCY DIAGRAM	25 -- EC+KBC (IT8502E)
06 -- POWER SEQUENCY TIMING	26 -- CODEC/JACK/SPEAKER/MIC
07 -- SMBUS MAP	27 -- LAN (RTL8103EL)/CLOCK GEN
08 -- Calpella (DMI,PEG,FDI)	28 -- Card Reader
09 -- Calpella (CLK,MISC,JTAG)	29 -- WLAN/BT/MDC/USB/MOUNTING
10 -- Calpella (DDR3)	30 -- LVDS/CRT/Webcam
11 -- Calpella (POWER/GND)	31 -- HDMI
12 -- Calpella (GRAPHIC POWER)	32 -- DCIN/Battery/OCP/FAN
13 -- PCH (HDA,JTAG,SATA)	33 -- PWR Charger MAX8731AETI
14 -- PCH (PCI-E,SMBUS,CLK)	34 -- 5V/3.3V SN0608098RHBT
15 -- PCH (DMI,FDI,GPIO,LVDS)	35 -- Vcore MAX17030
16 -- PCH (PCI,USB,NVRAM,GPIO)	36 -- 1.1V VTT/+V1.05RUN
17 -- PCH (POWER)	37 -- 1.5VDDR3+0.75V+V1.8RUN
18 -- DDR3(SO-DIMM_0&1)	38 -- PWR_Others power plane
19 -- VGA (PCI-E/STRAP) 1/5	39 -- CPU_VREG & Decoupling
20 -- VGA_S3 (IO) 2/5	40 -- ATVDD/+VPCIE


P. Leader	Check by	Design by

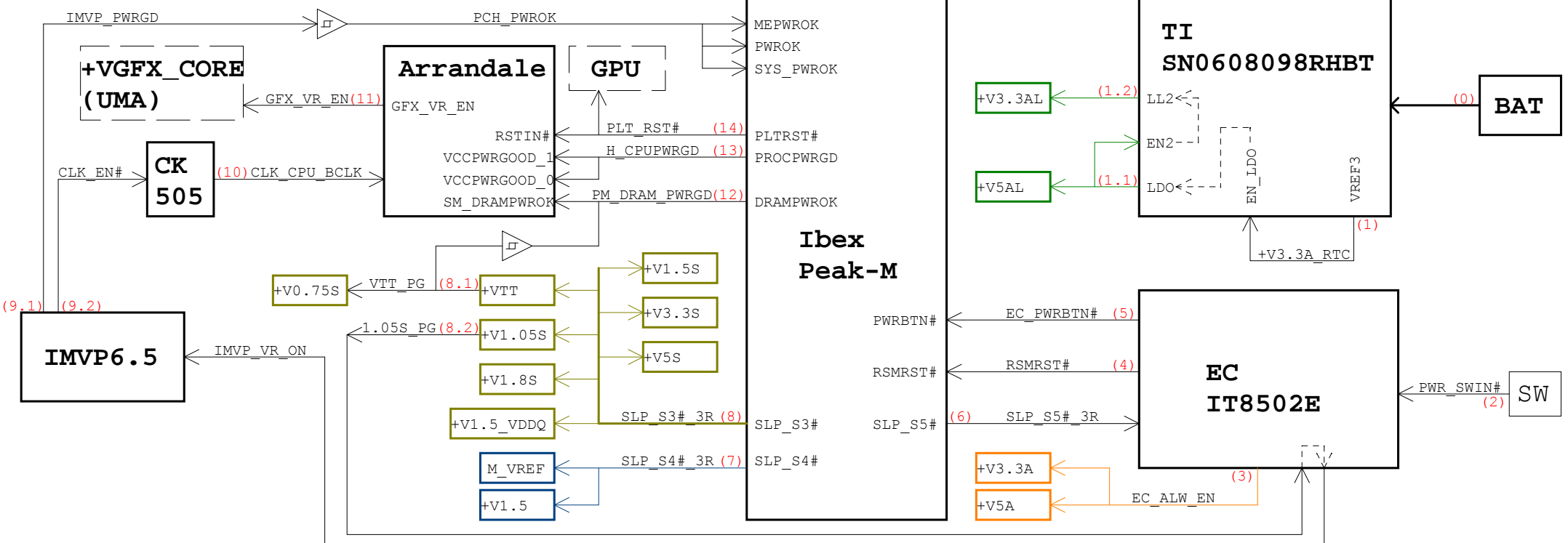
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Foxconn eMS Inc. HNBD R&D	
phone: +886-2-2799-6111	
Title Index Page	
Size Custom	Document Number STAR (Federer)
Page Modified: Thursday, March 18, 2010	17:24:40 (UTC+GMT) Sheet 1 of 40





SCH Page	Change Request Description	Notes
25,33~40	modify the power short pad to "POWER_OPENPAD_1P9X2P4"	SMD performance issue
15	Add RS74,RS77,RS79 for all SG sku	Fix VGA port auto detect function
39	Change PR944 from 1K to 1.5K	Fix power load line test issue
13	Del PCH SPI ROM connector circuitry	Del unnecessary functon parts
25	Del EC SPI ROM connector circuitry	Del unnecessary functon parts
25	Del debug connector	Del unnecessary functon part
25	SKU ID modify to MV phase	MV Phase ID
13	32.768KHZ crystal change to CL:7PF	RTC Clock tuning
25	32.768KHZ crystal change to CL:7PF	RTC Clock tuning
30	VGA connector change part number to halide free type	ROHS issue
29	MDC connector change part number to halide free type	ROHS issue
29	Mini-PCIE connector change part number to halide free type	ROHS issue
30	LVDS connector change part number to halide free type	ROHS issue
13	SATA connector change part number to halide free type	ROHS issue
30	Modify backlight PWM control path	Del unnecessary parts
18	Modify the DDR3 footprint	Co-lay for DDR3 connector
25	Del D110	Del unnecessary functon parts
25,30	Del RB28 and Add RI54	For 17" keyboard num lock LED
38	add PC775	Add for GPU M93 platform
38	add PC776	Add for VGA wave issue
35	Change VCORE VDD power source from +V5A to +V5S	Modify for V-BOOT
38	Change PR769 pull high power source from +12A to +V5A	Modify for GPU power sequence
29	Modify the HOLE1006 footprint	update footprint
40	modify all VDDCORE circuitry	modify VDDCORE circuitry
26	modify UA3 pin2 Analogy GND to Digital GND	Analogy GND change to Digital GND
32	add 2 pcs 2N7002 and swap EC_CHAR_LED#_A & EC_AC_LED#_W	Modify LED control and brightness
32	modify HEADER10 pin1 power source from +V5A to +V3.3AL	modify LED control and brightness
33~37	PC547 22uF_X5R_25V to 10uF_X5R_25V*2	modify for acoustic
	PC504 4.7uF_X5R_25V to 10uF_X5R_25V	
	PC813 4.7uF_X5R_25V to 10uF_X5R_25V	
	PC825, PC812 to 10uF_X5R_25V (NI)	
	PC826 to 10uF_X5R_25V (NI)	
	PC824, PC828, PC829 4.7uF_X5R_25V to 10uF_X5R_25V"	
32	RH1002 change to 1.3Kohm	modify LED control and brightness
27	RL13 change to 2.7Kohm"	modify LED control and brightness
32	ADD QB11	Thermal shutdown
19	ADD RG457,RG458	Add for power leakage issue
35	Del DB14	Thermal shutdown issue

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Title History			
Size	Document Number		Rev
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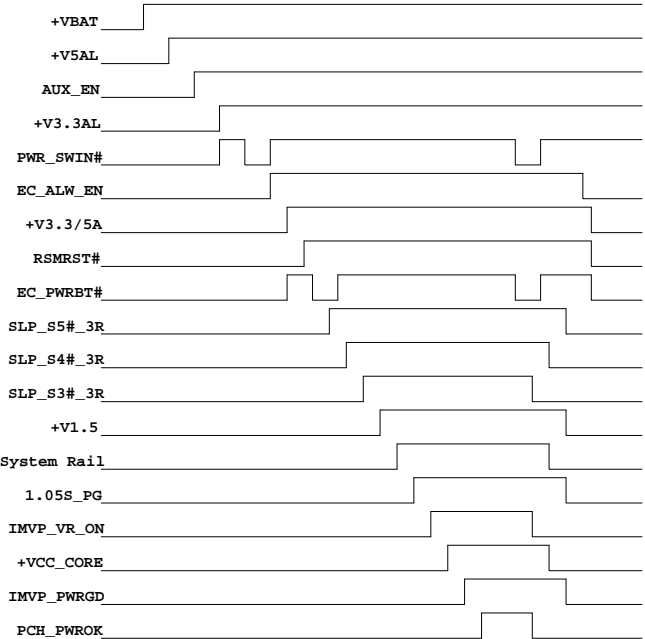


	Source Rail	EN	PG	Power Status				Remark
				S0	S3	AC S4/S5	DC S4/S5	
+VBAT	+VBAT	+V3.3A_RTC		V	V	V	V	
+V5AL	+VBAT	+V5AL		V	V	V	V	
+V3.3AL	+VBAT	+V5AL		V	V	V	V	
+V5A	+VBAT	EC_ALW_EN		V	V	V		
+V3.3A	+VBAT	EC_ALW_EN		V	V	V		
+V1.5	+VBAT	SLP_S4#_3R		V	V			
+V0.75S	+V1.5	VTT_PG		V				
+V1.5S	+V1.5	RUN_ON_LOAD		V				
+V1.5_VDDQ	+V1.5	RUN_ON_LOAD		V				
+VCC_CORE	+VBAT	IMVP_VR_ON	IMVP_PWRGD	V				
+VTT	+VBAT	SLP_S3#_3R	VTT_PG	V				
+VGFX_CORE	+VBAT	GFX_VR_EN		V				
+V1.8S	+VBAT	SLP_S3#_3R		V				
+V1.05S	+VBAT	SLP_S3#_3R	1.05S_PG	V				
+V5S	+V5A	RUN_ON_LOAD		V				
+V3.3S	+V3.3A	RUN_ON_LOAD		V				
+VDD_CORE	+VBAT	SLP_S3#_3R		V				
+V3.3S_Delay	+V3.3S	+V1.8S		V				
+VPCIE	+V1.5S	SLP_S3#_3R		V				

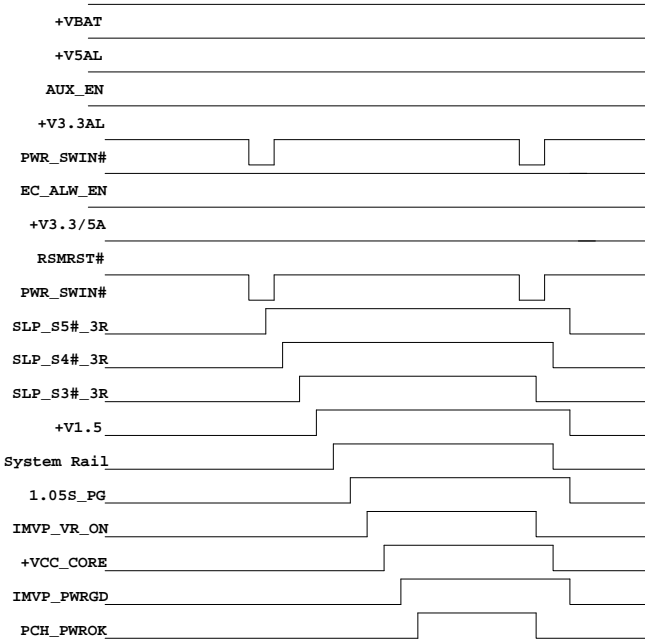
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POWER SEQUENCE TIMING

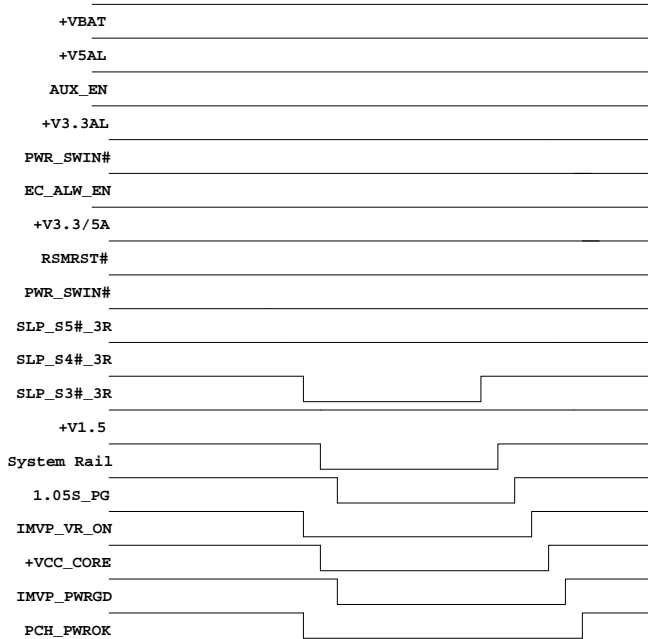
G3(OFF)->S0->S5



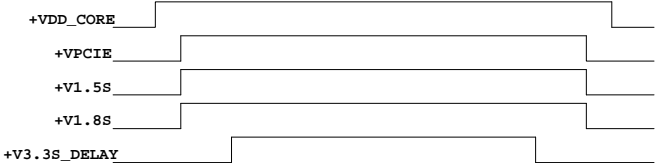
S5->S0->S5



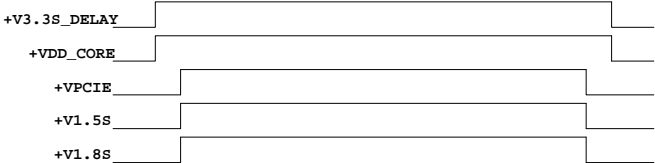
S0->S3->S0



GPU_M93 Sequence



GPU_Park Sequence



Switchable GPU

GPU
Park_XT

PCH

EC
ITE8502

DIMM0

DIMM1

CLOCK
GEN

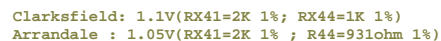
WLAN

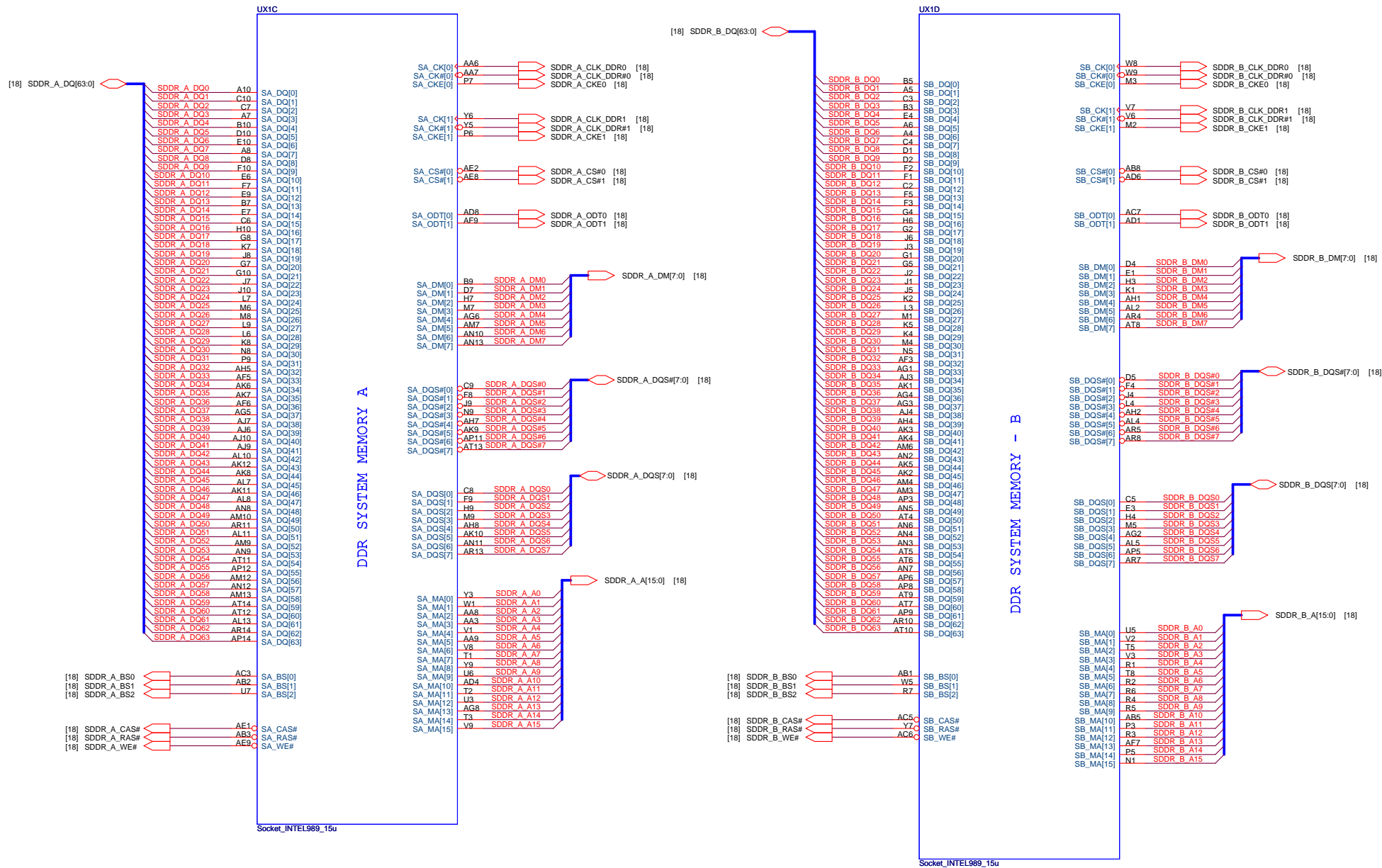
Temp
Sensor

Charger

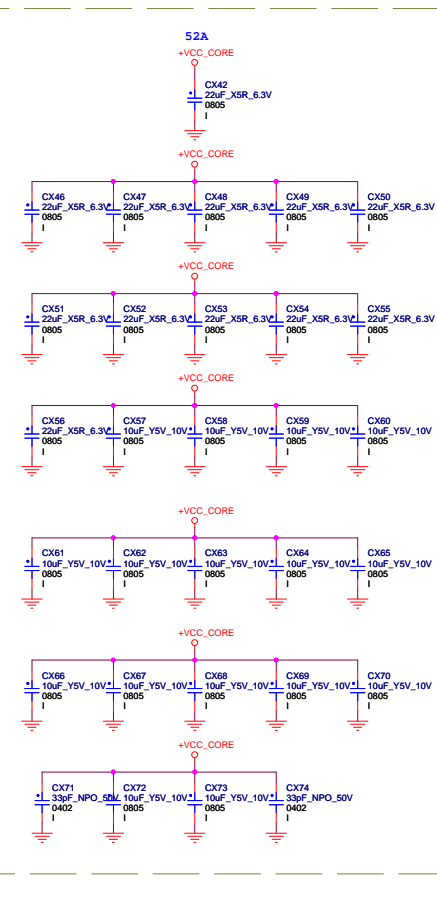
Battery

Place close to chip





FOR VCC:
12x 0805 22 μ F inside cavity,
7x 0805 10 μ F under cavity and 9 x 0805 10
 μ F
between inductor and socket on top layer



Socket_INTEL989_15u

POWER
CPU VIDS

SENSE LINES

PROC_DPRS_LPVRR

VTT_SELECT

ISENSE

VCC_SENSE

VSS_SENSE

VTT_SENSE

VSS_SENSE_VTT

VTT_SENSE_VTT

VSS_SENSE_VTT

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VSS_SENSE_VTT

VTT_SENSE_VTT

Arrandale drives this pin High
Clarkfield drives this pin Low.

Place close to CPU

FOR VTT:
7x 0805 22 μ F under
cavity
6x 0805 10 μ F edge caps

UX11

K27

K9

K6

J32

J30

J21

J19

H35

H32

H28

H26

H24

H22

H18

H15

H13

H8

H5

G34

G31

G20

G9

G8

G3

F30

F27

F25

F22

F19

F16

F13

F10

F7

F4

F1

E8

E5

D33

D30

D26

D23

D20

D17

D14

D11

D8

D5

D2

D1

C33

C30

C26

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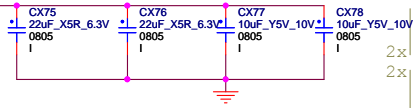
A14

A11

A

Discrete GPU: Install
UMA: Not Install

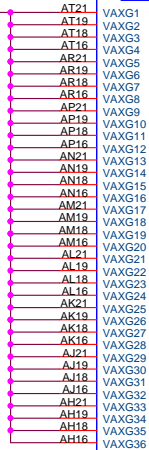
Max Current for Integrated Graphics Rail CCMAX_VAXG----22A



CX79

Discrete GPU: Not Install
UMA: Install

UX1G



GRAPHICS

POWER

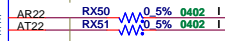
PDI

PBG & DMI

Socket_INTEL989_15u

+VTTQ [9,11,16,17,27,35,36,39]
+VGFX_COREQ [39]
+V1.5_VDDQ [9,17,27,29,38]
+V1.8S [17,37,38]

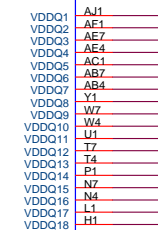
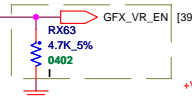
Discrete GPU: Not Install
UMA: Install



Discrete GPU: Install
UMA: Not Install

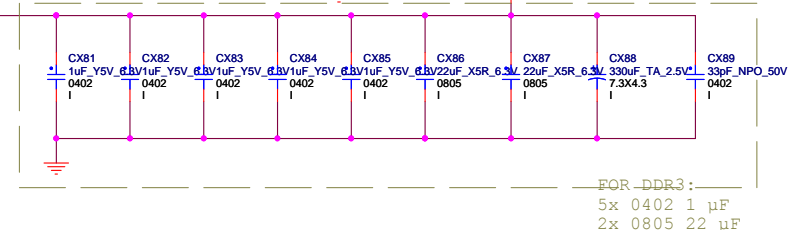


Discrete GPU: Not Install
UMA: Install

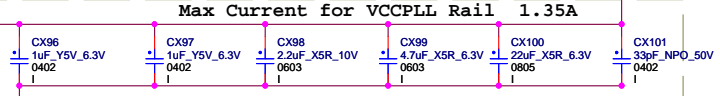
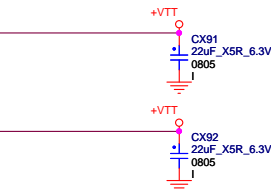
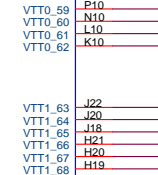


DDR3 - 1.5V RAILS

1.1V
1.8V



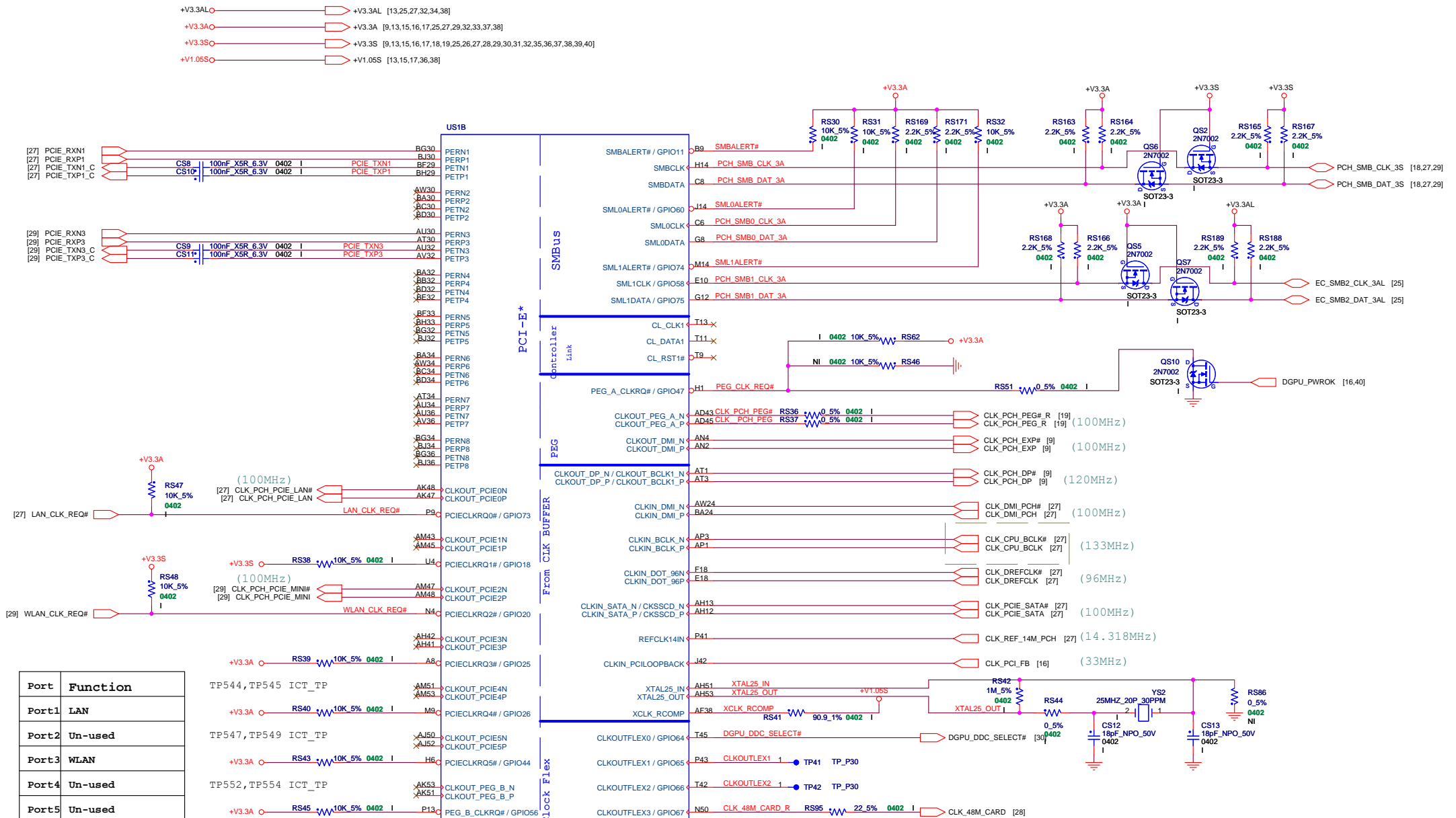
FOR_DDR3:
5x 0402 1 uF
2x 0805 22 uF



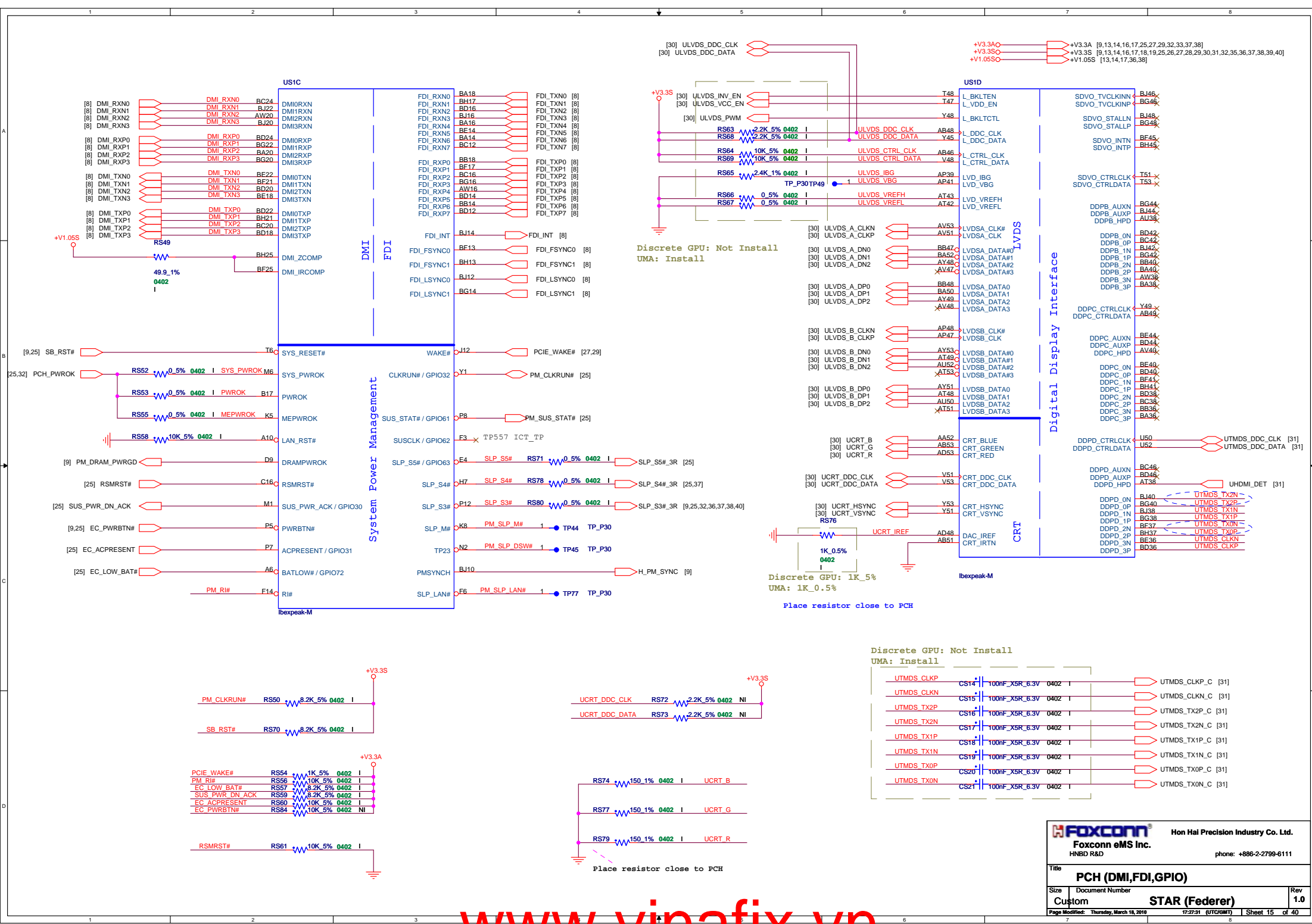
FOR_VCCPLL:
1x 0805 2.2 uF
2x 0805 1 uF
1x 0805 22 uF
1x 0603 4.7uF

Port	Function
Port1	LAN
Port2	Un-used
Port3	WLAN
Port4	Un-used
Port5	Un-used
Port6	Un-used
Port7	Un-used
Port8	Un-used

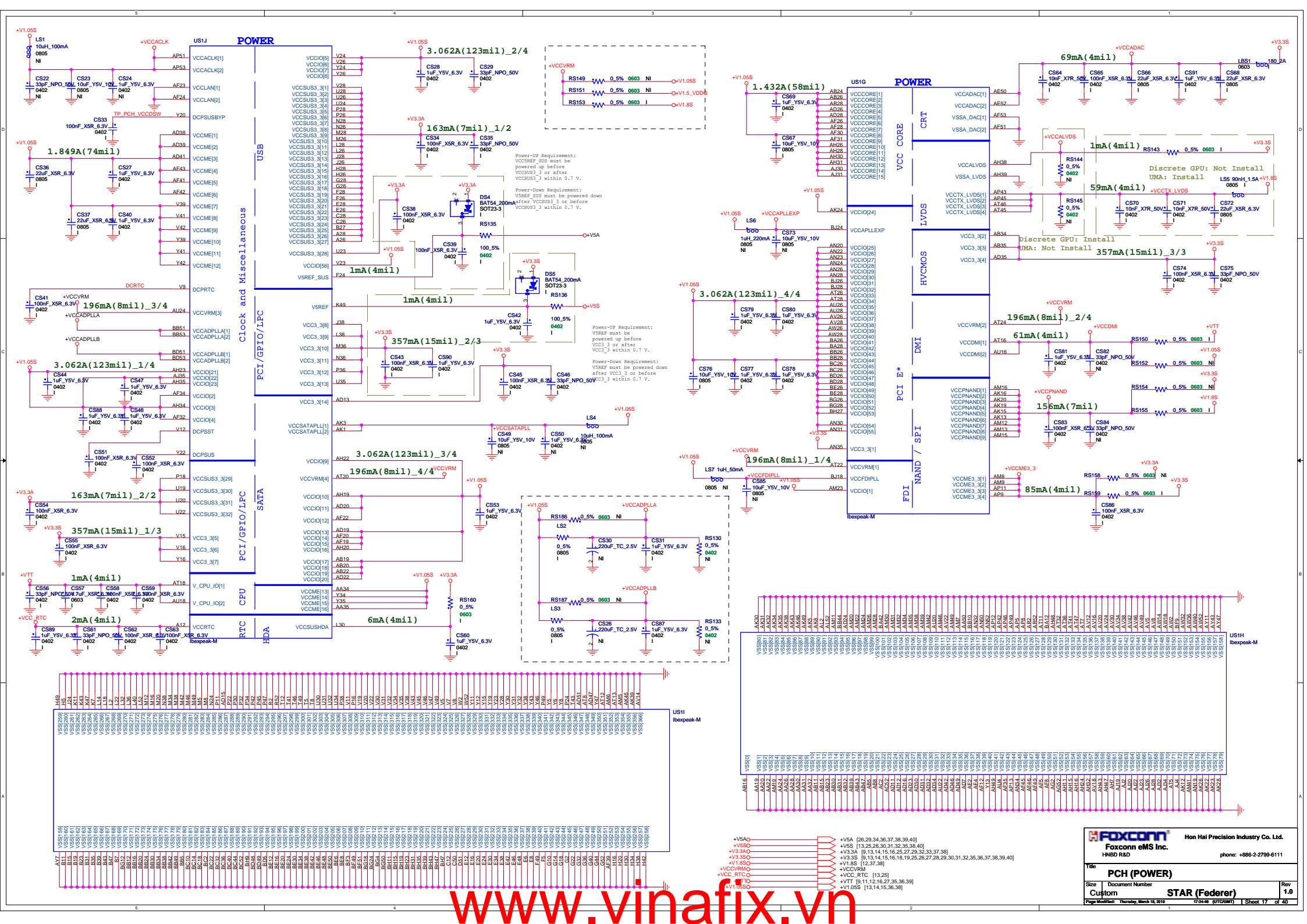
PCI-E Port Table




ibexpeak-M







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Time

PCH (POWER)

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Document Number

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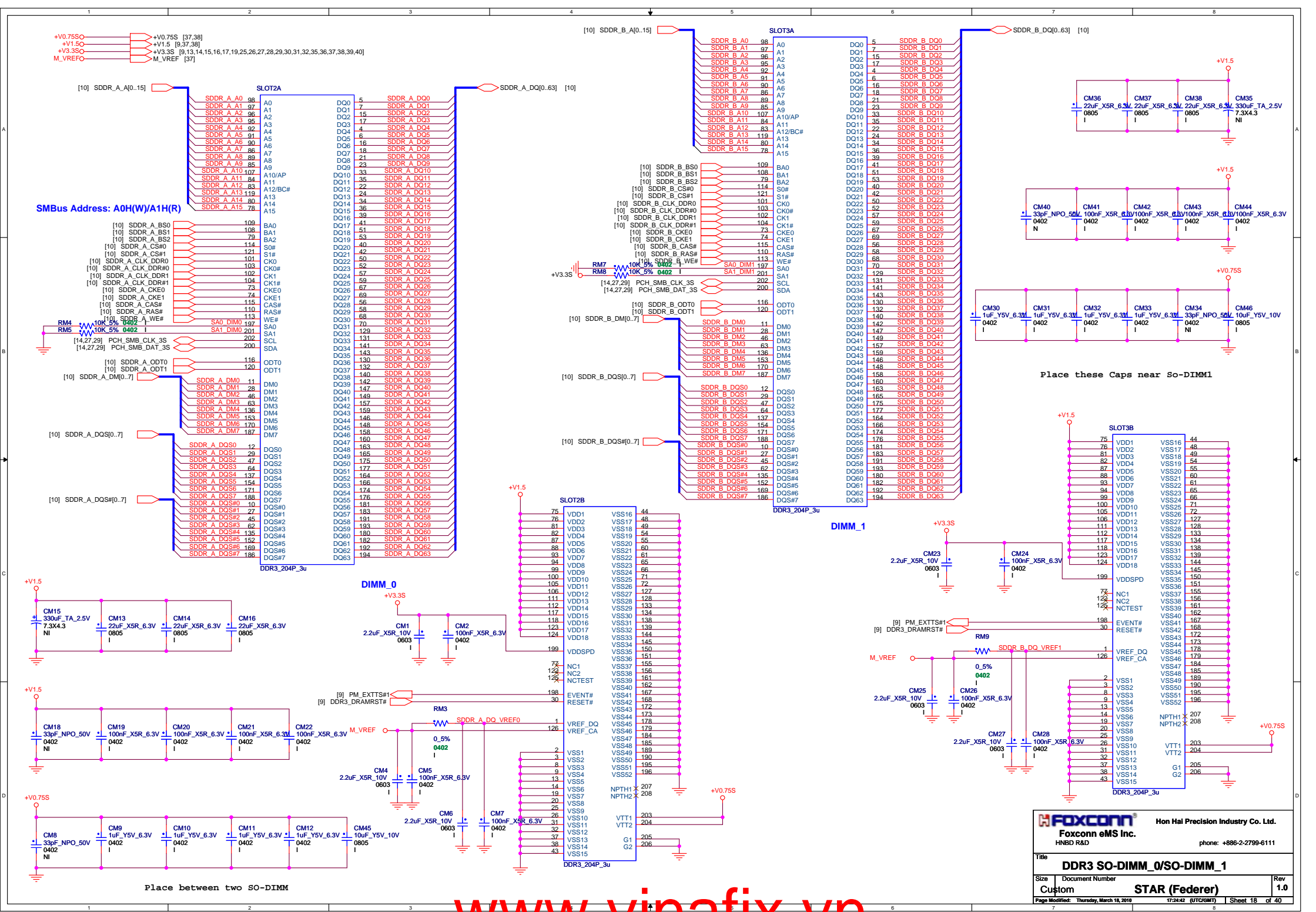
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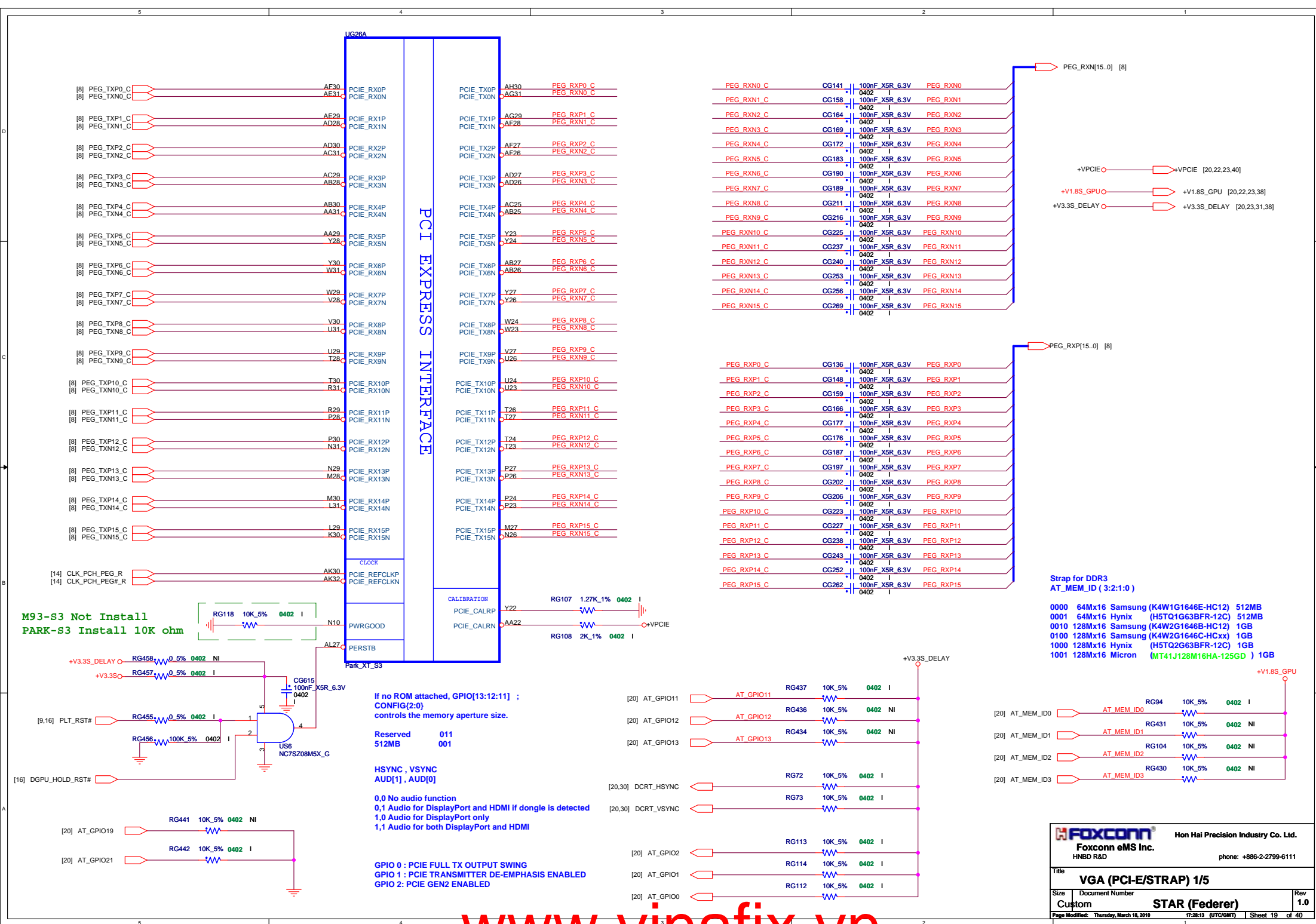
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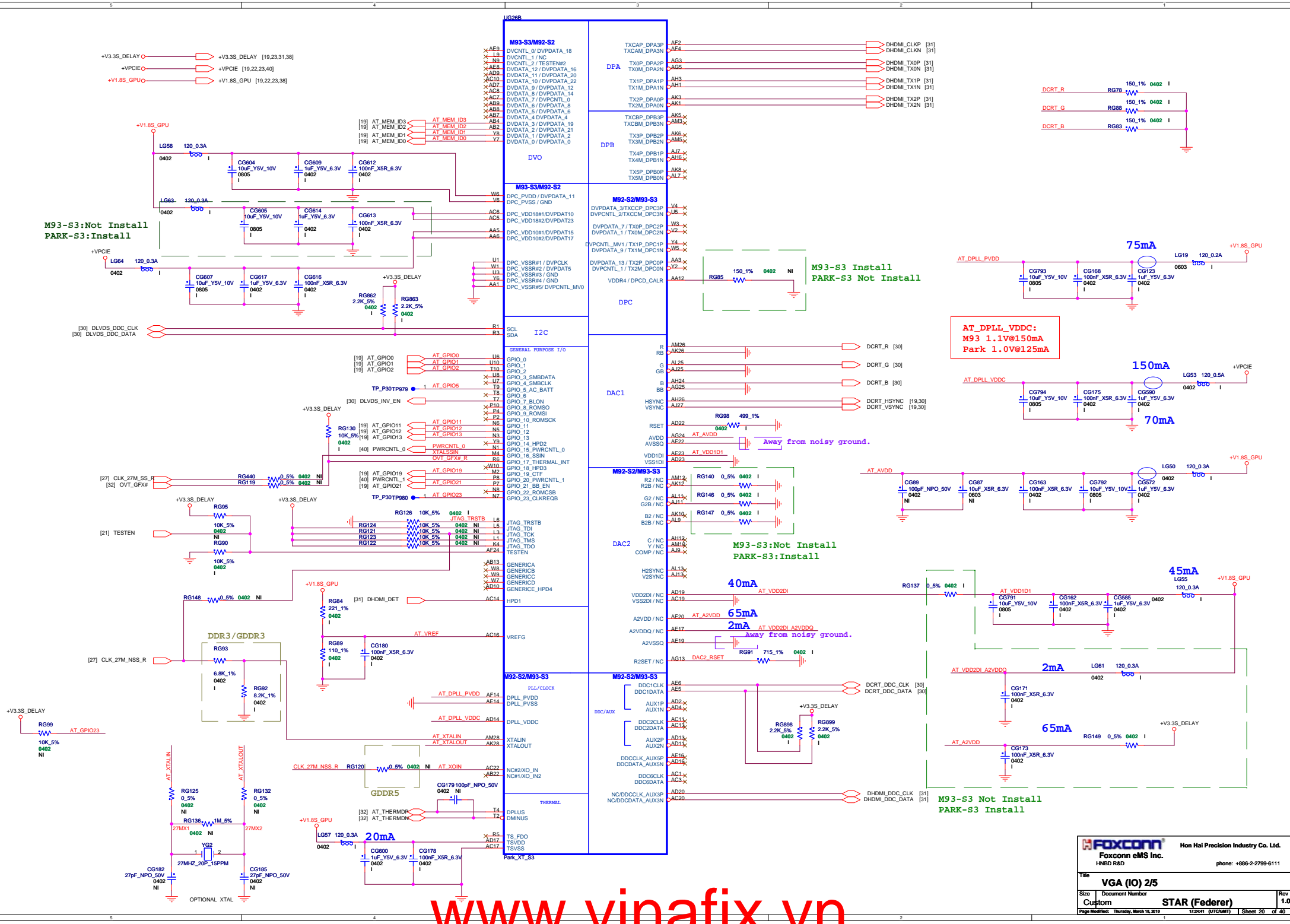
Sheet 18 of 40

Rev

1.0

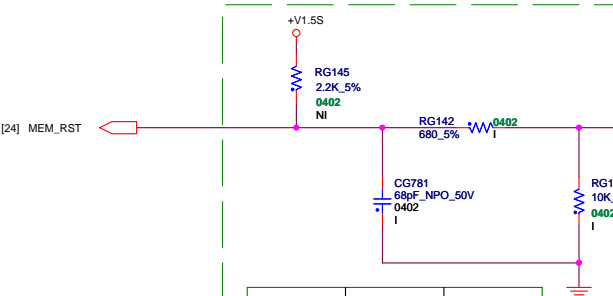
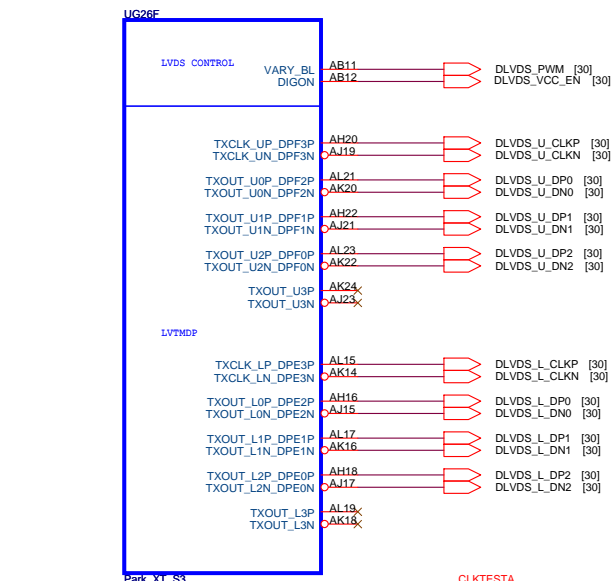






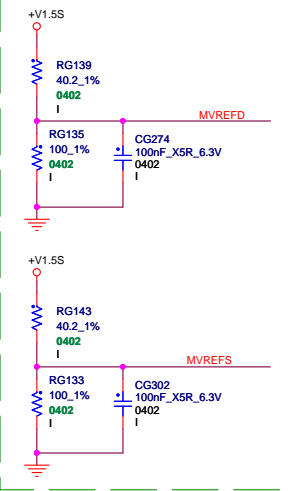
	M93_XT_S3	Park_XT_S3
RG139	100_1%	40.2_1%
MVREFD	0.75V	1.07V
RG143	100_1%	40.2_1%
MVREFS	0.75V	1.07V

+V1.5S

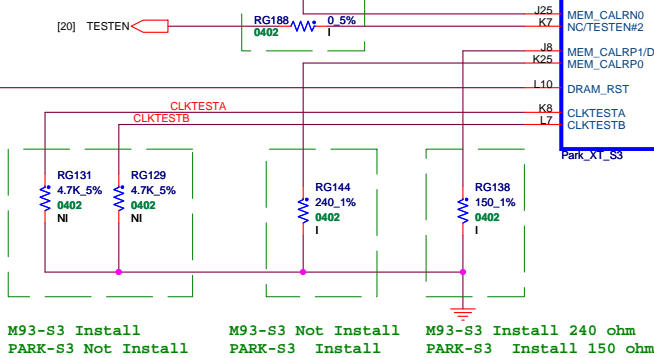


	M93-S3	PARK-S3
RG141	DNI	10K
RG142	0R	680R
RG145	2.2K	DNI
CG781	2.2nF	68pF

PLACE MVREF DIVIDERS
AND CAPS CLOSE TO ASIC

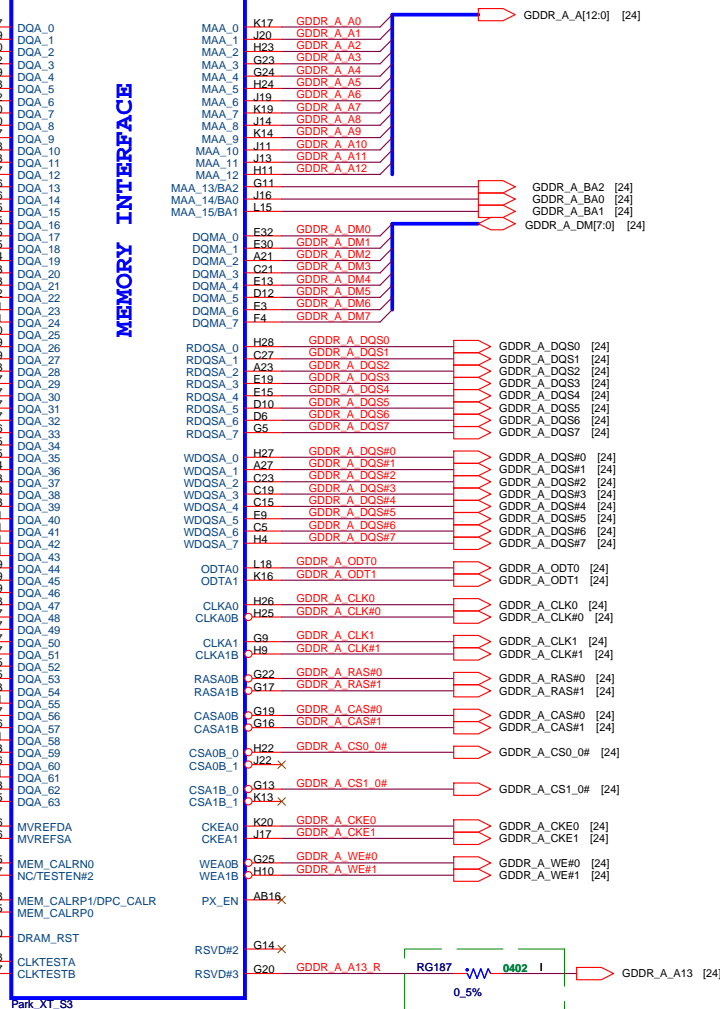


M93-S3 No Install
PARK-S3 Install



M93-S3 Install
PARK-S3 Not Install
M93-S3 Not Install
PARK-S3 Install
M93-S3 Install 240 ohm
PARK-S3 Install 150 ohm

UG26C

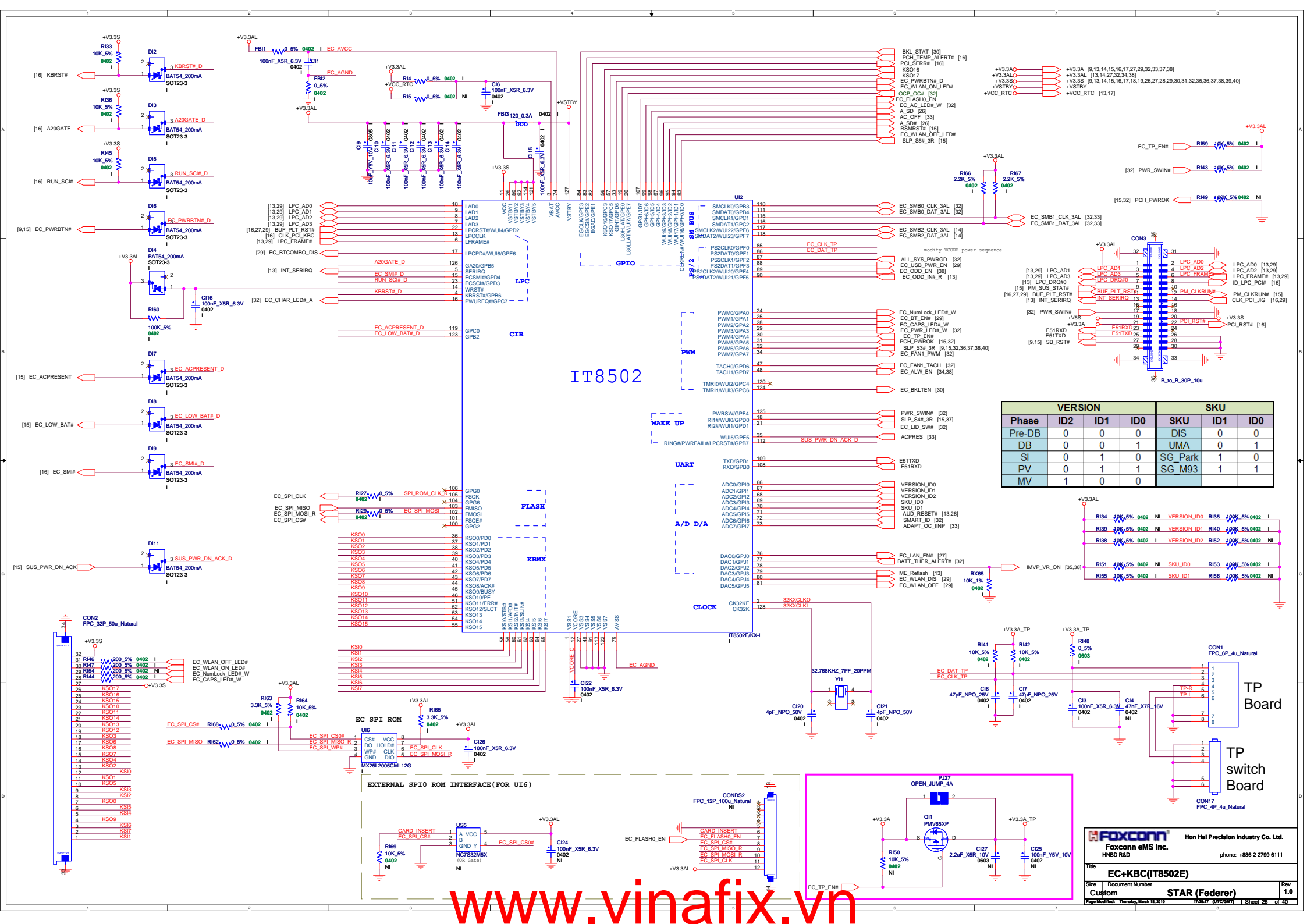


MEMORY INTERFACE

FOXCONN
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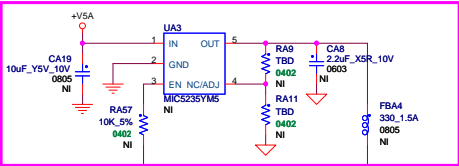
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Size: Document Number
Custom: **STAR (Federer)**
Page Modified: Thursday, March 18, 2010 17:34:42 (UTC+GMT) Sheet 21 of 40

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VERSION				SKU		
Phase	ID2	ID1	ID0	SKU	ID1	ID0
Pre-DB	0	0	0	DIS	0	0
DB	0	0	1	UMA	0	1
SI	0	1	0	SG Park	1	0
PV	0	1	1	SG M93	1	1
MV	1	0	0			

Reserved LDO circuitry for +VDDA power source



Place next to pin 38

Split by DGND

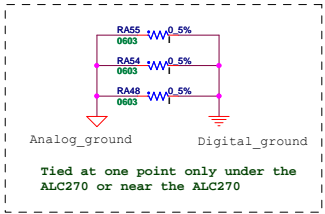
Split by DGND

Split by DGND

<<Attention>>
Surges of PVDD >7V duration 0.1ms when class D amplifier is working may damage the amplifier, 10uF tantalum capacitors are required at PVDD1 and PVDD2 to suppress the surge

A_SD# = 0V:
Power down Class D SPK amplifier

A_SD# = 3.3V:
Power up Class D SPK amplifier



ALC270A-GR
(Viate Premium Version)
Thermal Pad
6 x 6 mm
9 Via Array

ANALOG
DIGITAL
(Include Thermal Pad)

With Microphone Pre-AMP

Reserved for without Microphone Pre-AMP

PC BEEP

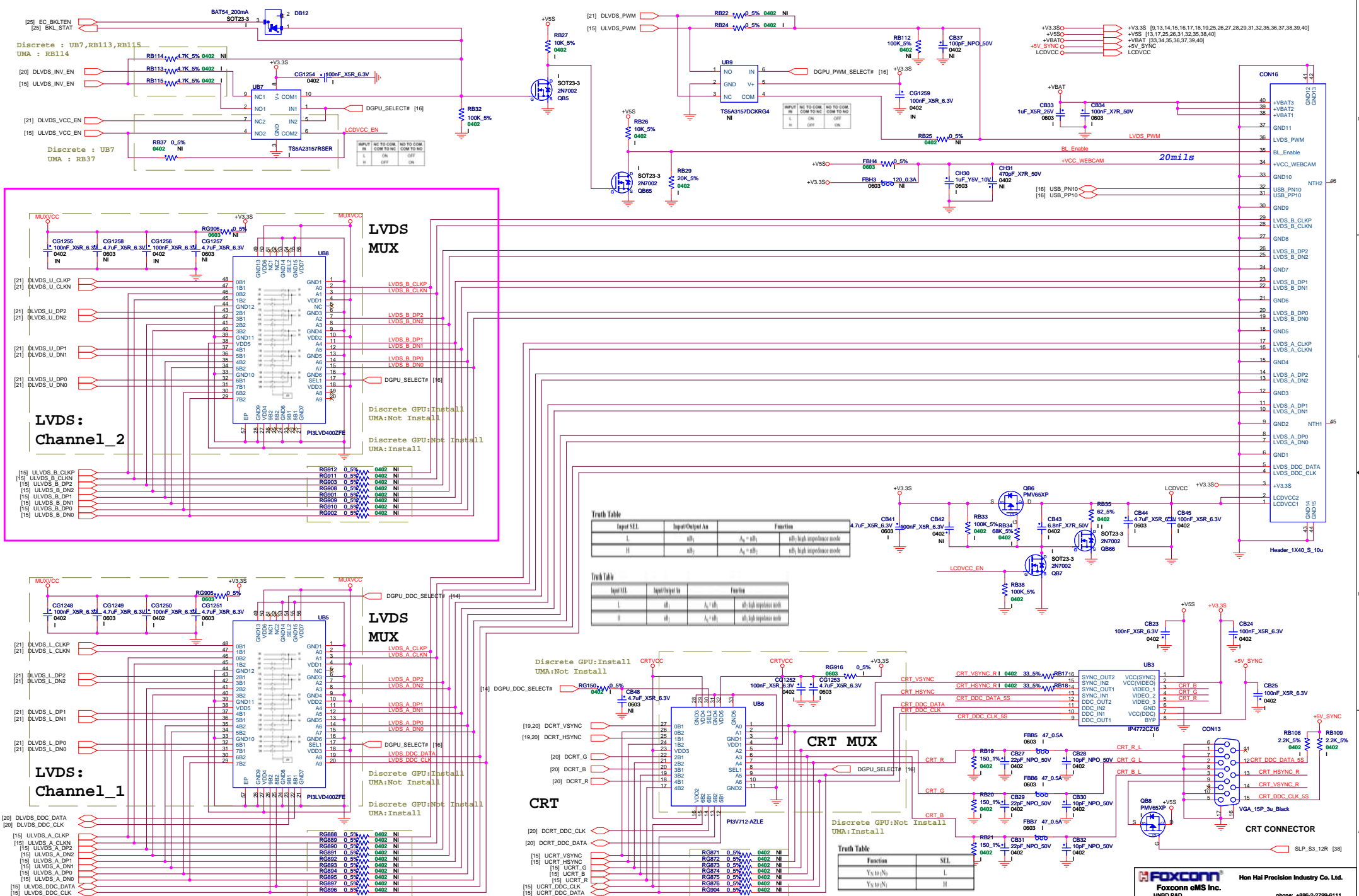
INTERNAL MICROPHONE

INTERNAL SPEAKER

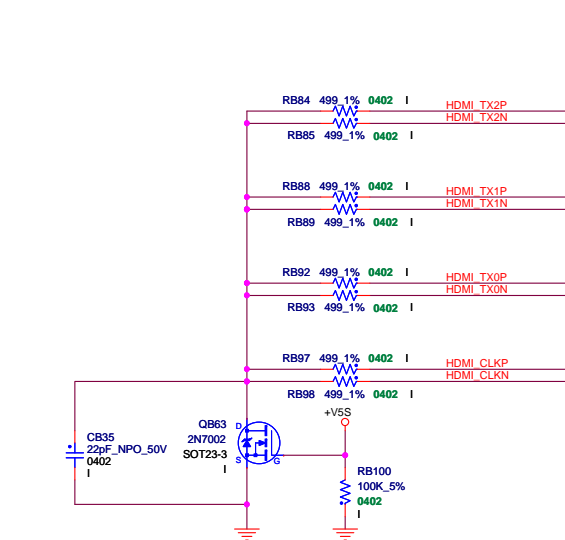
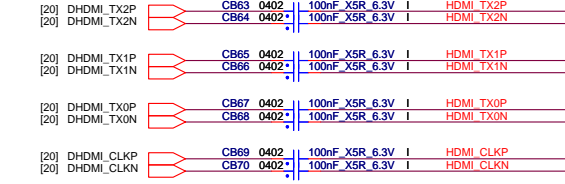
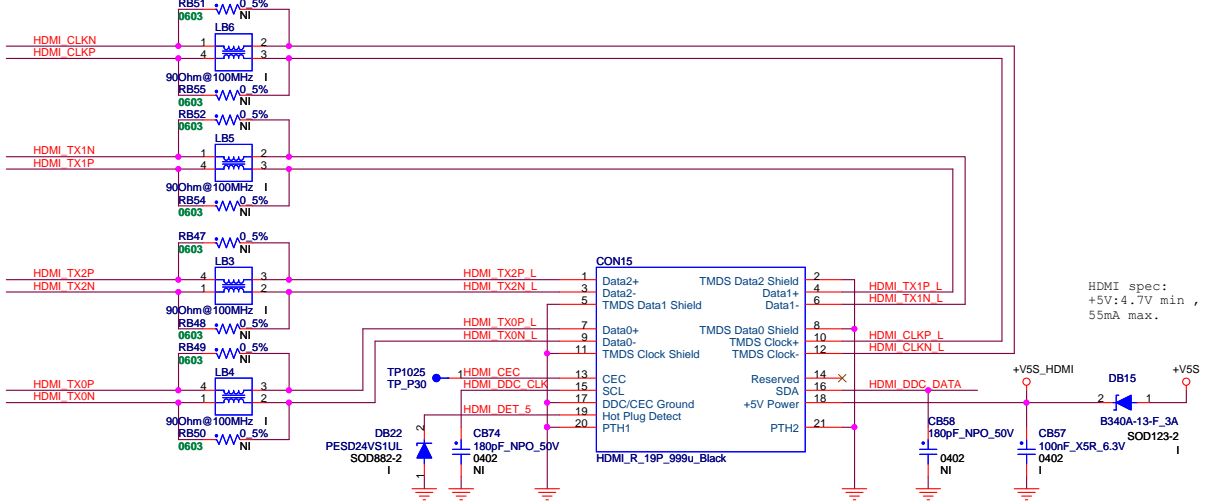
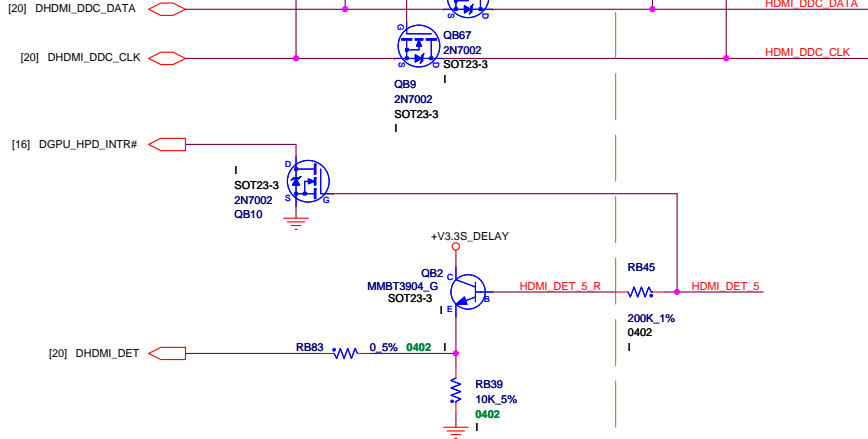
EXTERNAL MIC Jack

HEADPHONE Jack

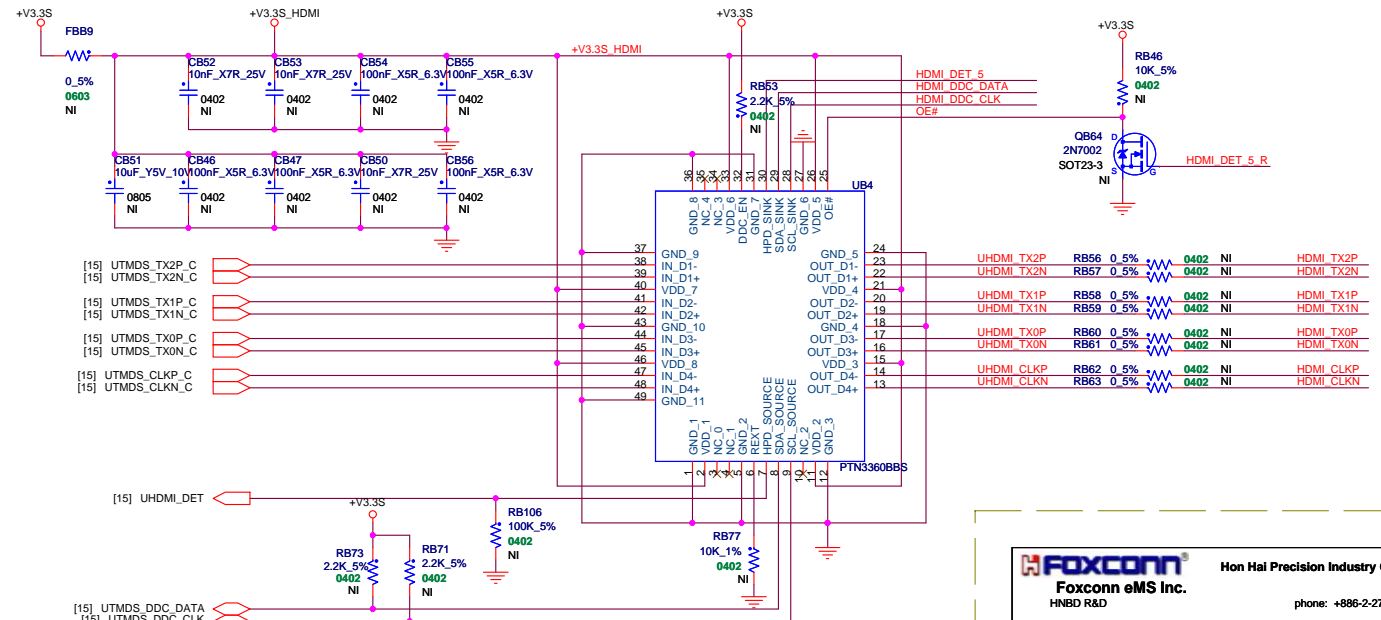




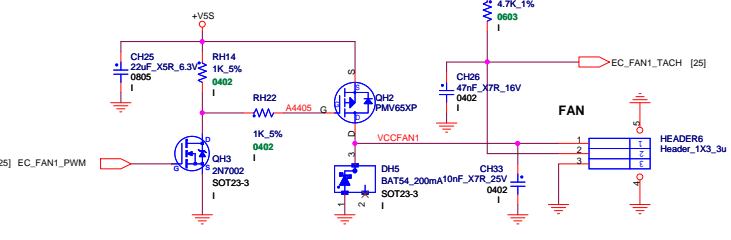
Discrete GPU: Install
UMA: Not Install



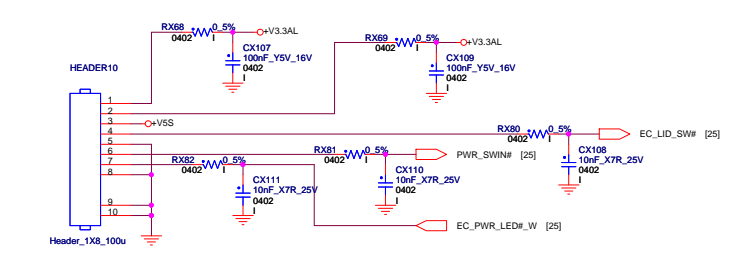
Discrete GPU:Not Install
UMA:Install



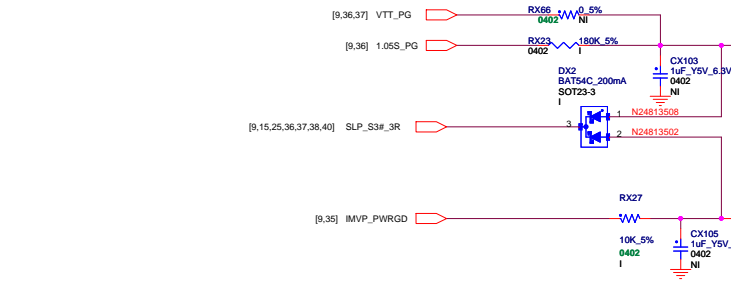
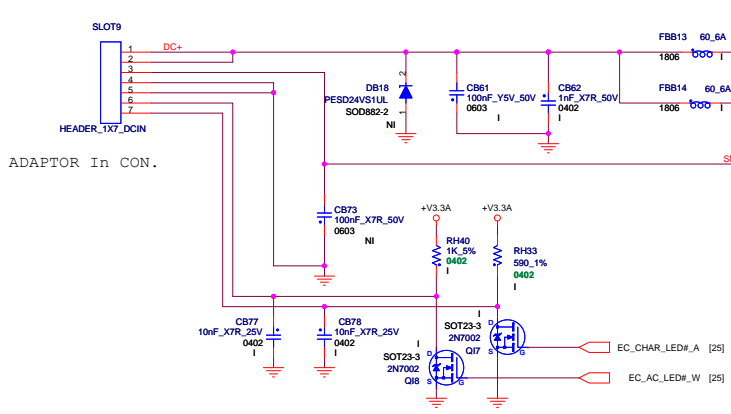
FAN CONNECTOR



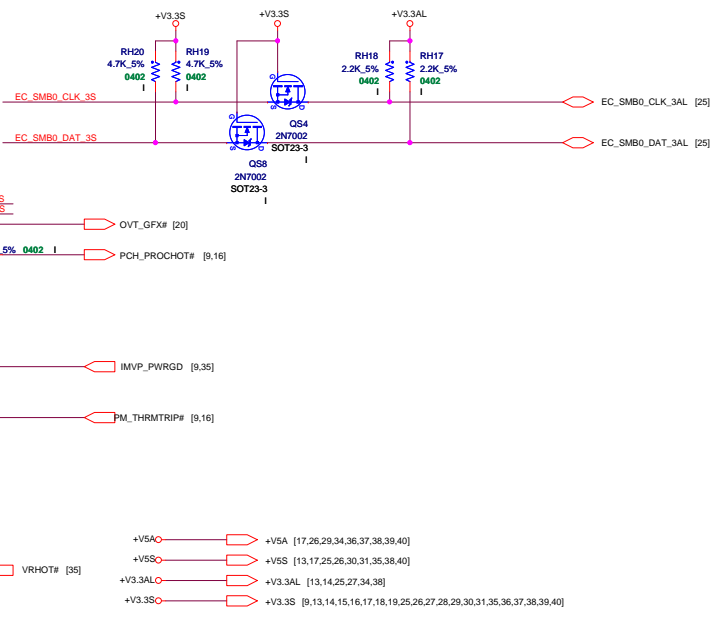
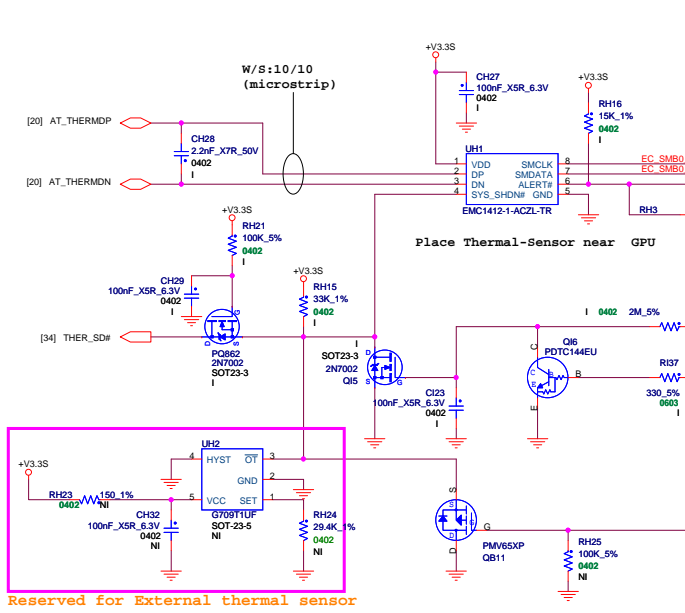
POWER BUTTON BOARD CONNECTOR



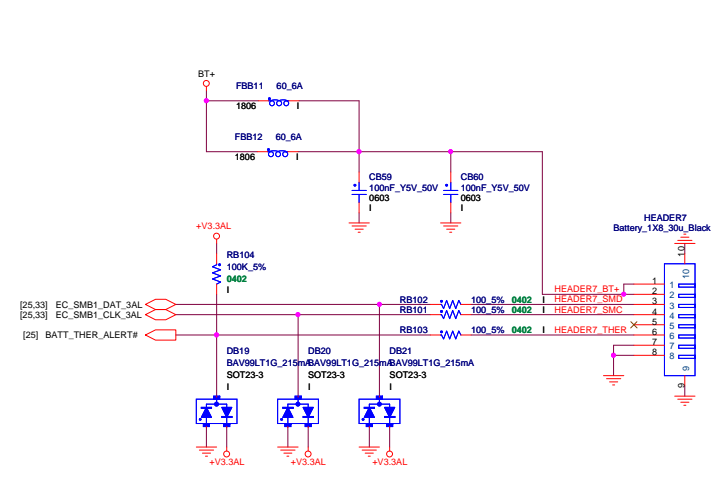
DC_JACK Wire to Board Connector



THERMAL SENSOR



BATTERY CONNECTOR



Pin No.	Symbol	Comments
1	BATT+	Batt+, Battery Positive Terminal
2	BATT+	Batt+, Battery Positive Terminal
3	SMD	SMbus data interface I/O pin.
4	SMC	SMbus clock interface I/O pin
5	ID	Open
6	B/I	Connect to Blemar (103A72 equivalent)
7	GND	Batt-, Battery Negative Terminal
8	GND	Batt-, Battery Negative Terminal

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Title

DCIN/Battery/OCF/FAN

Size

Document Number

Custom

STAR (Federer)

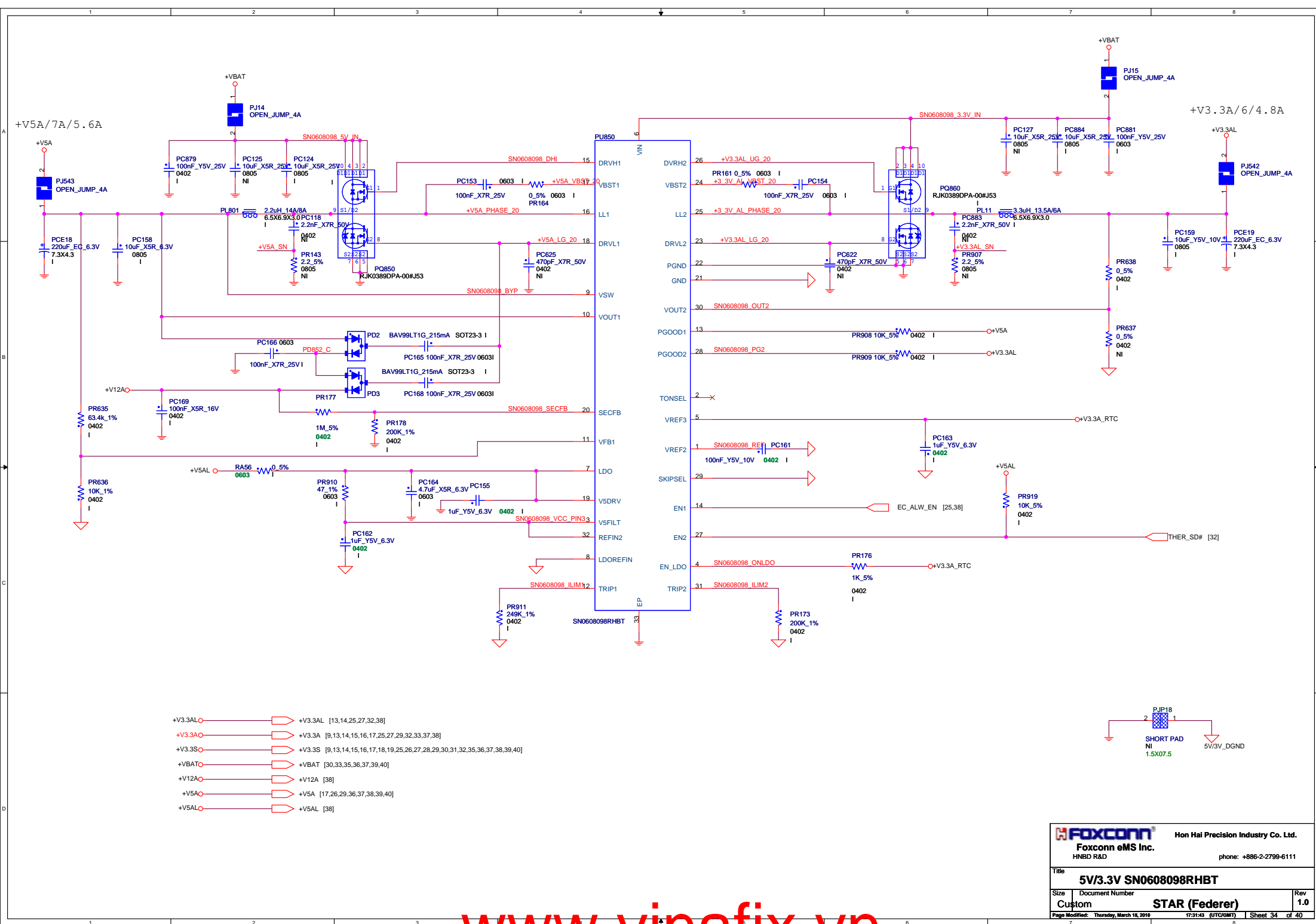
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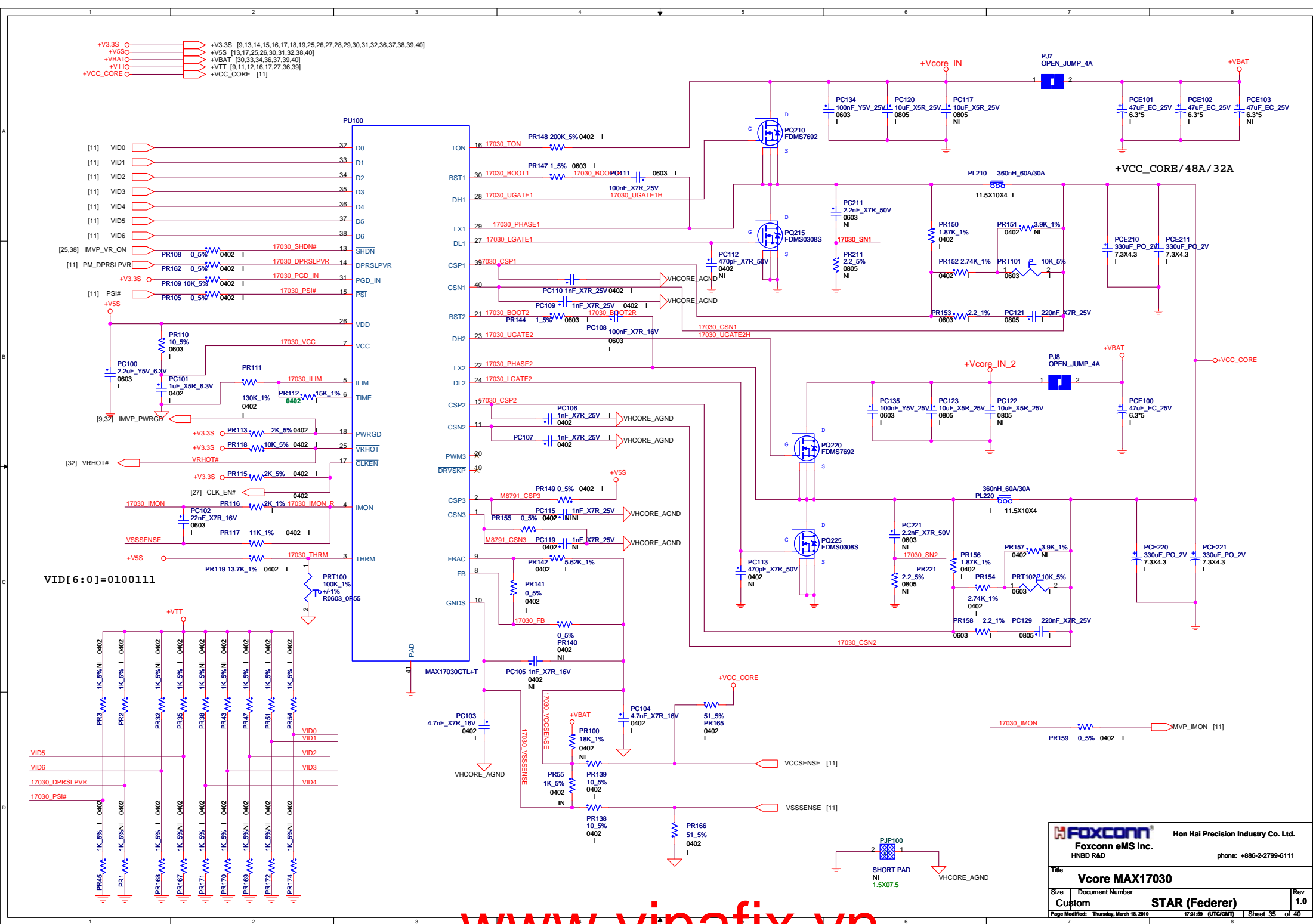
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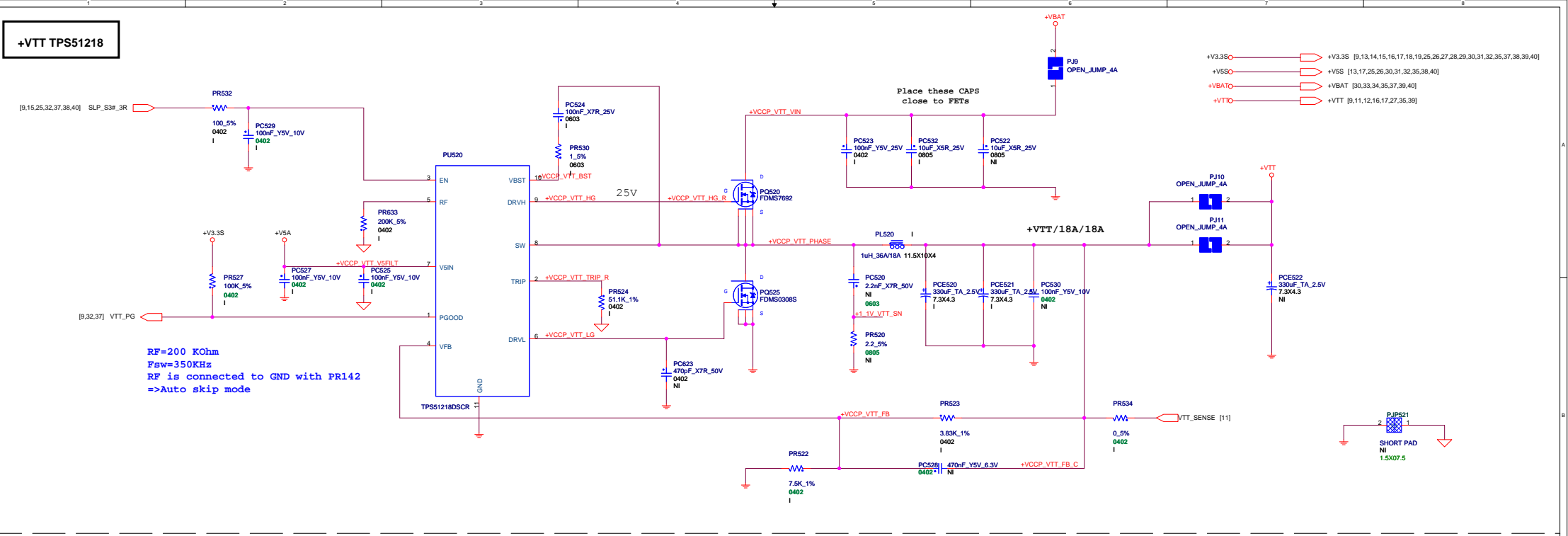




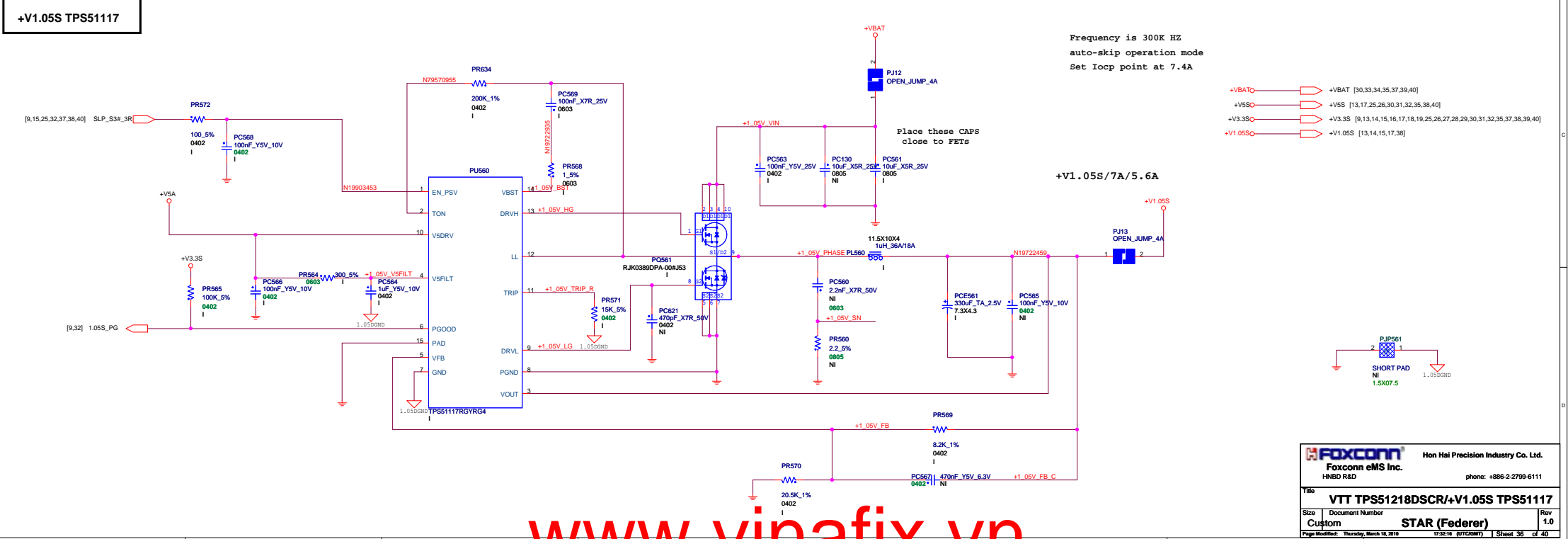
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